A FAST FREQUENCY SWITCHING SYNTHESIZER WITH AN INTEGRATION CIRCUIT

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ABSTRACT

A new type of direct frequency synthesizer which can complete frequency switching in less than a microsecond is proposed. This yields low-spurious outputs by low-power analog integration circuit whose operating principle is similar to a digital accumulator. Experimental results confirm successful frequency synthesizer operation.

INTRODUCTION

Fast frequency switching of frequency synthesizers has become an important requirement in spread spectrum and other wireless communication systems. Direct digital synthesizers (DDSs) are able to provide the required fast frequency switching because they have no feedback loop, such as that used in phase locked loop (PLL) frequency synthesizers. DDSs have certain disadvantages, however, such as narrow tuning bandwidths and large power consumption. The most popular DDS is the sine output DDS [1], the tuning bandwidth of which is limited by the ROM access time. Since the use of larger ROM increases both ROM access time and power consumption, efforts have been made to reduce ROM size without degrading the spurious performance [2], [3]. In an attempt to achieve a high-speed, low-power frequency synthesizer, we have already proposed two types of ROM-less DDSs, namely a DDS with an interpolation circuit [4], and a DDS with digitally controlled delay generator [5]. Both ROM-less DDSs have potential for realizing a high-speed, low-power frequency synthesizer, however a high-speed digital circuit, which includes an accumulator, consumes a lot of power.

This paper presents a new concept of direct frequency synthesis, using an analog integrator to create the same waveforms that the digital accumulator creates with an interpolation circuit. This synthesizer outputs square waves with low spurious components. A digital resetting circuit is adopted to restrain frequency drift in the output signal. Experimental results confirm the validity of the concept.

PRINCIPLE

A digital accumulator which consists of a full adder and a latch is shown in Fig. 1(a) and a timing chart of output data θ,

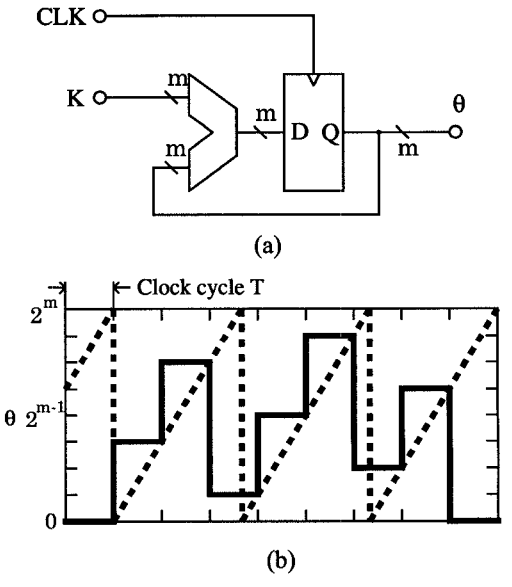

Fig. 1 Accumulator and its operation.
(a) circuit configuration
(b) timing chart

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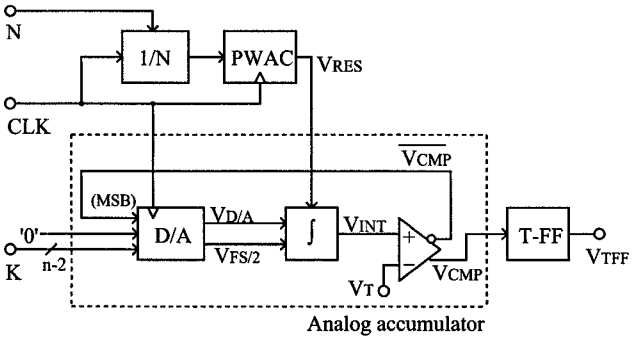

Fig. 2 Proposed frequency synthesizer.

for bit size m = 3 and frequency control word K = 3, is shown in Fig. 1(b). The hypothetical sawtooth waveform shown by the dotted line in Fig. 1(b) is ideally periodic. This waveform can be generated by an accumulator with an interpolation circuit [4]. Here we propose a new frequency synthesizer which creates the hypothetical sawtooth waveform without the digital accumulator.

The block diagram of the proposed frequency synthesizer is shown in Fig. 2. The frequency synthesizer consists of an n-bit digital-to-analog converter (D/A), an integrator, a voltage comparator, a frequency divider, a pulse width adjusting circuit (PWAC), and a toggle flip-flop (T-FF). Division ratio of the

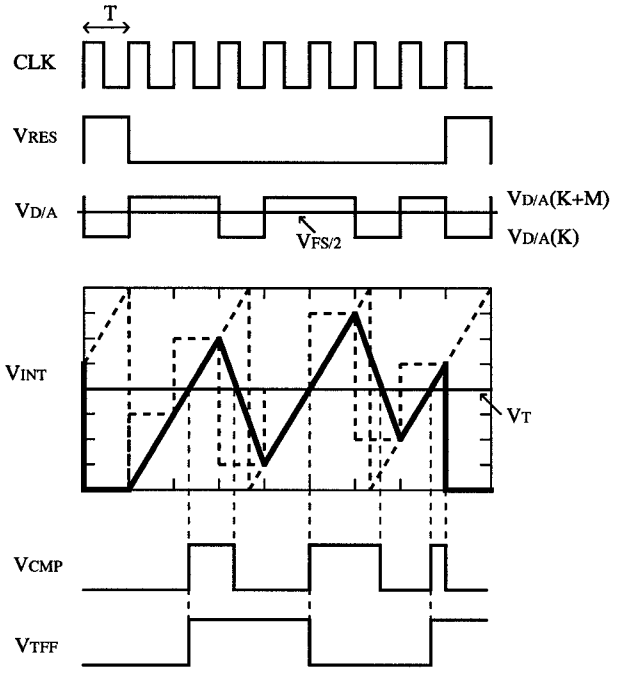

Fig. 3 Waveforms of the frequency synthesizer.

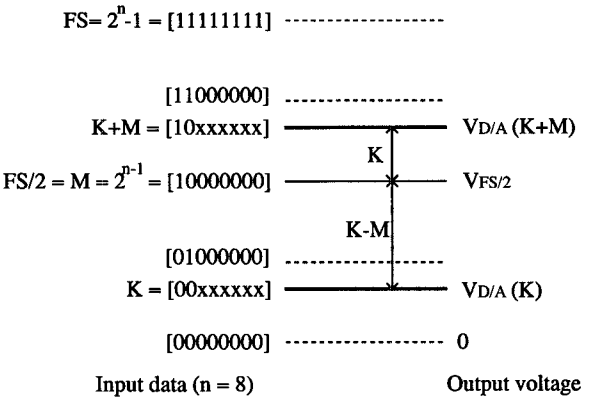

Fig. 4 Output voltages of the D/A.

frequency divider, N, can be chosen from the relation:

$$N = L\,\frac{M}{G}\,, \tag{1}$$

where G is the greatest common divisor (g. c. d.) between K and M (= 2^{n-1}), and L is an integer greather than or equal to one.

The waveforms of the frequency synthesizer are shown in Fig. 3 for resolution of the D/A n = 4 (namely M = 8), frequency control word K = 3 and division ratio N = 8. The PWAC output, V_{RES}, contains one pulse within a period of N·T, where T is clock cycle. The pulse width of V_{RES} is adjusted to be T by the PWAC. The D/A output, $V_{D/A}$, varies its voltage between two levels, $V_{D/A}$ (K) and $V_{D/A}$ (K+M), which are proportional to K and K + M respectively. Figure 4 shows the relation of $V_{D/A}$ and $V_{FS/2}$, where $V_{FS/2}$ is a constant voltage proportional to M (the median voltage in the D/A). The integrator integrates the differential voltage, $V_{D/A} - V_{FS/2}$. The PWAC output, V_{RES}, resets the integrator periodically. This initialization reforms the integrator output, V_{INT}, which is assumed to drift easily. V_{INT} agrees with the hypothetical sawtooth waveform shown in Fig. 1(b). The timing of coincidence of V_{INT} and a threshold voltage, V_T, is detected by the voltage comparator as rising edges of the pulses from the voltage comparator, V_{CMP}. Because the period when V_{INT} decreases is one clock cycle for $K < 2^{n-2}$, the intervals of rising edges of V_{CMP} pulses are constant. The T-FF output, V_{TFF}, becomes a square waveform with duty cycle of exactly 50% when the T-FF operates at the rising edge of the input signal. The fundamental frequency is given by

$$f_{TFF} = \frac{1}{2}\,\frac{K}{M}\,f_{CLK}\,, \tag{2}$$

where f_{CLK} is the clock frequency. The T-FF can be replaced by

a one-shot multivibrator that operates at the rising edge of the input signal. In this case, the fundamental frequency of the synthesizer output is given by twice (2).

Compared with DDSs, including ROM-less DDSs, this frequency synthesizer is expected to reduce power consumption dramatically. The circuit scale of the analog part and the D/A are similar to the ROM-less DDS [4], however, the gate number of the digital part, which dominates the power consumption in the synthesizer, is considerably reduced in comparison with the DDSs. An m-bit accumulator, which is used in DDSs, consists of an m-bit full adder and an m-bit latch, and all gates operates at clock frequency. On the other hand, a binary counter, which is used in this frequency synthesizer, consists of several T-FFs, but only one T-FF operates at the clock frequency and the other T-FFs operates at lower frequencies. This means that at a given clock frequency, this frequency synthesizer can operate at much lower power than a DDS.

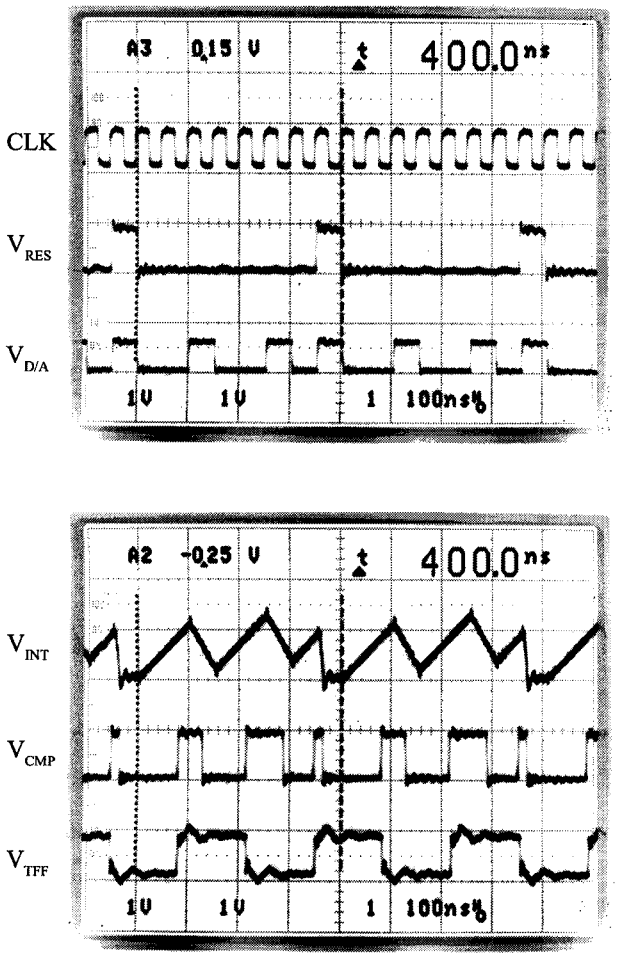

Fig. 5 Waveforms.

EXPERIMENTAL RESULTS

The synthesizer shown in Fig. 2 was achieved by combining discrete components. In this experiment, an 8-bit D/A (n = 8) and a 4-bit binary counter were employed. Here, $V_{FS/2}$ is supplied

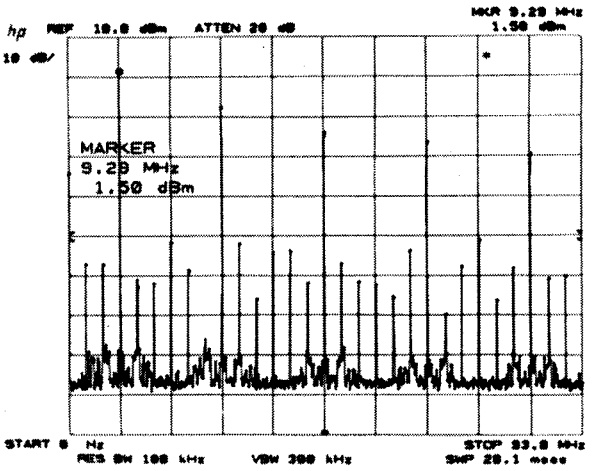

Fig. 6 Spectrum of the frequency synthesizer output, V_{TFF}. H: DC-93.8 MHz; V: 10 dB/div.

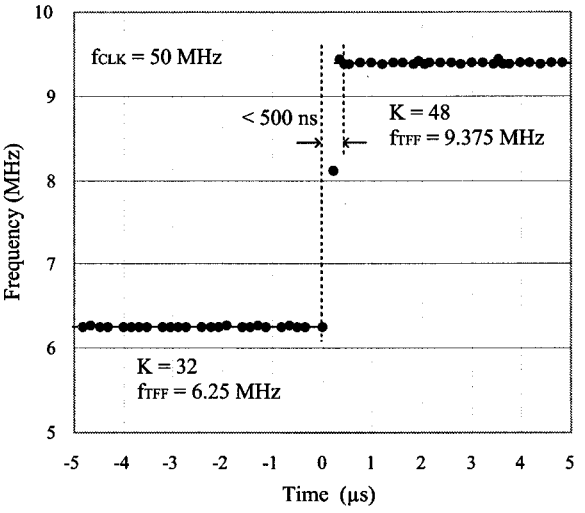

Fig. 7 Time dependence of output frequency during frequency switching.

by a programmable power source. Figure 5 shows waveforms of the synthesizer measured on an oscilloscope. The signal symbols on the left side correspond to those in Fig. 3. Note that the polarity of $V_{D/A}$ is different from that in Fig. 3. The clock frequency, f_{CLK}, is 20 MHz and the frequency control word, K, is 48, hence the fundamental frequency of the synthesizer output, f_{TFF}, is expected to be 3.75 MHz. Division ratio of the frequency divider, N, is selected to be 8. Figure 5 shows that the integrator output, V_{INT}, is similar to the hypothetical sawtooth waveform shown in Fig. 1(b). Figure 5 also shows that the synthesizer output, V_{TFF}, is a square waveform with duty cycle of exactly 50%. Figure 6 shows the spectrum of the synthesizer output, V_{TFF}, for the frequency control word K = 48 and with a higher clock frequency f_{CLK} = 50 MHz. The spectrum of V_{TFF} includes the fundamental frequency, 9.375 MHz, and its harmonics, and the highest spurious level, excluding the harmonics, is –45 dBc. Figure 7 shows the time dependence of output frequency during frequency switching, as measured by a frequency and time interval analyzer (HP5372A). The frequency control word K = 32 corresponds to the output fundamental frequency 6.25 MHz, and K = 48 corresponds to 9.375 MHz. This result shows that the frequency switching is completed within less than 500 ns.

We are now integrating an 8-bit DAC (with $V_{FS/2}$ output) with a high-speed Si bipolar process [6]. This DAC can operate at a 1-GHz clock input. Proposed frequency synthesizer is expected to be used for local oscillators in microwave communication equipments. For high frequency applications, an up-converting technique can be applied using a constant-frequency microwave signal generator.

CONCLUSION

A new direct frequency synthesizer has been developed. Experimental results show that the frequency synthesizer creates square waves with low spurious components. The digital resetting circuit, which consists of the frequency divider and the PWAC is effective in restraining frequency drift in the output signal. The proposed architecture can be applied to high-speed and low-power frequency synthesizers for wireless communication systems that require fast frequency switching.

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